REMARKS

These remarks are in response to the third, non-final Office Action mailed on November 11, 2001. The Office Action rejected claims 1-42, with claims 1-3, 8, 12-16, 19-21, 25, 36, 39 and 40 under 35 U.S.C. 102(a) as being anticipated by Kayanuma et al. (U.S. patent number 5,397,729), claims 26, 27 and 30 under 35 U.S.C. 102(a) as being anticipated by Takahashi et al. (U.S. patent number 5,618,749), and the remaining claims under 35 U.S.C. 103(a) with one of these two patents as the primary reference. All of these rejected claims are believed allowable for the reasons described below and are discussed in groups according to order in the Office Action.

Claim 17 was also rejected under 35 U.S.C. 112, second paragraph. Claim 17 has now been amended to add a "prior" that was erroneously omitted from its original form. Applicants thank the Examiner for noting this omission.

The Office Action objected to the drawings under 37CFR 1.83(a) for not showing the etching of the bottom of the electrode. This feature is found in independent claim 1 and its dependent claims, claims 2 and 12, as described in the embodiment using the flow beginning on line 1 of page 9 of the present application. Newly added Figure 12 is a flow chart of this flow and presents the same information as shown there. As such, it introduces no new matter. The lower electrode etch is step 13 of this flow. The new figure has also been appropriately referenced in the Specification in a way to introduce no new matter.

35 U.S.C. 102(a) Rejections based on Kayanuma *et al.*(U.S. Pat. No. 5,397,729)

The Office Action rejected claims 1-42, with claims 1-3, 8, 12-16, 19-21, 25, 36, 39 and 40 under 35 U.S.C. 102(a) as being anticipated by Kayanuma et al. (U.S. patent number 5,397,729). These rejections are respectfully submitted to be in error. The Kayanuma patent will be briefly discussed first as it is believed that this digression will facilitate the follow explanation of why this patent does not anticipate the rejected claims.

Kayanuma presents a method for forming a capacitor, but the emphasis there is on incorporating metal silicides into the process, this focus being reflected in the patent's title. As the Office Action notes, a lower electrode layer, inter-plate insulating layer, and upper electrode are all formed, with the upper electrode being defined by an etch. (The patent also

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

notes that "the insulating layer 53 may also be etched", although it does not indicate by how much or to what purpose and, in particular, does not teach etching to expose the lower electrode layer.) Subsequently, an insulating layer (57 in Figure 4C) is formed over the resultant structure and defined (Figure 4D), followed by the formation of the metal silicide layer (59 in Figures 4E). The purpose of the metal silicide is to reduce the resultant resistance of the gate structure (52 and 59 over region 55 in Figure 4F); the purpose of the oxide layer 57 is to protect the capacitor from the metal silicide.

Metal silicides are used as a treatment with metal to reduce resistance in polysilicon and employed in smaller devices for this purpose, as noted in the Office Action's comments with respect to claims 10, 23, and 29 and 11, 24, and 30. Although they will grow on silicon, they do not form on an oxide layer. More importantly in the present discussion, they are not an anti-reflective layer, but rather increase reflectivity.

The Takahashi patent discussed below does refer to "refractory metal silicides", for example at column 8, lines 8-13. However, refractory is a term used to indicate the material can withstand high temperatures, that is, it has a high melting point. What defines "high" in this context depends on the nature of the process: in the case of silicon CMOS processing titanium, tungsten or examples named in the Kayanuma patent are refractory metals. The term "refractory" has no connection to optical properties in this context, but rather material properties.

The silicides are used for the top layer on the gate structure (59 at the right of Figure 4F) to improve its properties. However, according the teachings of Kayanuma, to protect the capacitor plates, the oxide layer is formed over the entire capacitor structure and maintained there during entire processing involving the metal silicides. This can be seen in Figures 4D-4F where the oxide 57 is maintained over capacitor structure on the left while the gate is formed, thereby helping to maintain the electrical integrity of the capacitor structure.

Consequently, the Kayanuma patent differs from, and does not anticipate, the present invention as presented in the pending claims. More particularly, with respect to claim 1, claim 1 recites "forming a conformal insulating layer..." over the capacitor structure as shown in the embodiment of Figures 2-5 of the present application. In contrast, the structure the Office Action cites as corresponding to the "conformal insulating layer" of the application is the silicon oxide layer 57 described at column 8, lines 48-57, of Kayanuma. As described at the cited location, this oxide layer has "a thickness of, for instance, 1,000Å", that is, a fairly thick oxide layer as opposed to the sort of thinner conformal oxide layer found in the

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

embodiment of the present invention shown in Figures 2-5 of the present application. Additionally, as noted above, the Kayanuma patent does not describe etching the dielectric layer "to expose a portion of said lower electrode layer". Consequently, is respectfully submitted that the Kayanuma patent does not anticipate claim 1 on the present application and that a rejection of claim1 and its dependent claims, claims 2 and 12, under 35 U.S.C. 102(a) is not well founded. As discussed below with respect to claim 4, not only is it respectfully submitted that Kayanuma does not teach the conformal layer of claim 1, but that it is contrary to the purposes of Kayanuma.

With respect to claim 3, the Office Action identifies the metal silicide layer (59) with the anti-reflective layer of claim 3. As noted above, metal silicides are *not* anti-reflective, but, in contrast, tend to increase reflectivity. Consequently, the rejection of claim 3 and its dependent claims 8-10, is respectively submitted to be in error and that theses claims are allowable over the prior art. Claim 8 is further believed allowable as the metal silicides are further not an anti-reflective coating.

(Claim 9, that is discussed further below, does employ titanium nitride (TiN) containing the metal titanium, but is not a metal silicide. In contrast to the silicides, TiN can be employed as an anti-reflective layer. In the Office Action's comments with respect to claims 10, 23, and 29 and 11, 24, and 30, titanium *silicide* appears to be confounded with titanium *nitride*.)

Claim 13 is drawn to the embodiment of the present invention shown in Figures 6-9 that employs side wall spacers (185 of Figures 8 and 9) and contains the language "forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric". In contrast, the method of Kayanuma maintains a dielectric layer (57) over the top of the entire capacitor structure, as shown there in Figures 4D-4F. As discussed above, this is needed to protect the capacitor from the metal silicides used in Kayanuma. A side wall spacer arrangement, such as described in claim 13 and shown in Figures 6-9 of the present application, is not only not taught by Kayanuma but would be contrary to its purposes as it would leave the top electrode exposed to the subsequently formed metal silicide layer. Additionally, it again noted that Kayanuma does not describe etching the dielectric layer to expose the lower electrode. Consequently, claim 13 and its dependent claims, claims 14-25 are believed allowable and that the 35 U.S.C. 102(a) rejection based on Kayanuma is not well founded.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

Claim 15 and its dependent claims, claims 16-25, are further believed allowable as the cited metal silicide layer is not an anti-reflective layer, as discussed above.

With respect to claim 20, the cited locations refer to the combined *thickness* of layers 53 and 57. There is no disclosure of a side wall nor its *width* in the cited reference. Claim 21 is further believed allowable as the metal silicides are further not an anti-reflective coating.

Concerning independent claim 36, this contains both the anti-reflective layer and the conformal insulating layer. Consequently, based on these features, claim 36 and its dependent claims, claims 37-39, are believed allowable for the reasons described above.

Claim 40 is drawn to the feature that the flow is designed so that the capacitor module is removable without altering the other portions of the flow: "whereby said ARL is additionally formed over said capacitor structures, and whereby said conformal insulating layer is formed such that said provided process flow is unaltered...". There is no indication of such a limitation in the Kayanuma reference. As already noted, the Office Action mis-identifies the metal silicide layer as an anti-reflective layer, which is not disclosed in the Kayanuma patent. Additionally, the Kayanuma patent does not use a conformal insulating layer, but rather the thicker oxide layer 57. The Kayanuma patent also does not describe the capacitor formation process being such that the process flow without the formation of a capacitor being unaltered when the capacitor formation process is included. Kayanuma only describes t a flow that includes the capacitor formation. More specifically, by including the sort of insulating layer 57 as described in Kayanuma, a new process would be needed to compensate for the thickness of this layer. Consequently, the rejection of claim 40 is respectfully submitted to be in error and it believed that claim 40 and its dependent claims, claim 41-42, are allowable.

35 U.S.C. 102(a) Rejections based on Takahashi *et al.*(U.S. Pat. No. 5,618,749)

The Office Action rejected claims 26, 27 and 30 under 35 U.S.C. 102(a) as being anticipated by Takahashi *et al.* (U.S. patent number 5,618,749). The last part of claim 26 reads:

> ....removing a portion of said top electrode layer to expose a portion of the dielectric layer;
>
> forming an anti-reflective layer (ARL) over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

This differs from the process found in Takahashi. The Takahashi patent again uses a metal silicide layer, that the Office Action again identifies with the anti-reflective layer of the claim; as already discussed above with respect to the Kayanuma patent, metal silicides are not anti-reflective layers and tend to increase reflectivity. Takahashi presents no teachings on the use of anti-reflective layers.

(The Takahashi patent seeks to apply the metal silicide to the top electrode of the capacitor as well as the transistor gate, thereby forming both a polycide electrode and a polycide gate. This is different than Kayanuma, where the capacitor electrodes are protected from the metal silicide when the gate receives this treatment. In either case, though, a metal silicide layer is used to improve conductivity and is not a anti-reflective layer.)

Also, as seen in Figures 7-9 of Takahashi, both the top electrode layer (6a) and the inter-poly dielectric (1) are both etched away to the lower electrode (2), with the metal silicide layer (6b) placed over the top and bottom electrode layers, the dielectric layer having been removed except between these two layers. In contrast, the present invention as presented in claim 26 removes part of the top electrode layer, but leaves an exposed dielectric over which the anti-reflective layer is formed, *followed* the dielectric layer being etched.

For any of these reasons, claim 26 and its dependent claims, claims 27-30, are believed allowable. Claim 27 is further believed allowable as Takahashi further does not teach an anti-reflective coating, the metal silicide layer being neither anti-reflective nor a coating.

Rejections under 35 U.S.C. 103(a)

The Office Action rejected claims 4-7, 9-11, 17, 18, 22-24, 29-35, 37, 38, 41, and 42 under 35 U.S.C. 103(a) with either Kayanuma or Takahashi as the principle reference. Aside from claims 31-35, these claims all depend on claims discussed above and are consequently believed allowable as their base claim is believed allowable as discussed above. A number of these claims are believed further allowable for the reasons given below. Independent claim 31 and its dependent claims, claims 32-35, are also believed allowable.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

These rejections are discussed below in the order in which they are dealt with in the Office Action.

Concerning claim 4, the Office Action notes that Kayanuma does not disclose an insulating layer in the thickness range of 20-70Å and introduces Wang for this value. As noted above in the discussion of Kayanuma, the purpose of the insulating layer introduces there is solely for the protection of the capacitor electrodes and a thickness of 1000 Å, over an order of magnitude greater than the 20-70Å range, is used. It respectfully submitted that it is not obvious to combine these references in this way as the purpose in Kayanuma is to ensure the capacitor is well protected and using such a thin layer is contrary to this purpose. In contrast, the present invention seeks to maintain the optical properties while maintaining electrical integrity. Concerning claim 6, the Office Action states "[i]t is well known in the art" to use the values found in the claim without providing a reference and consequently it is respectfully submitted that a *prima facie* case has not been made. Therefore, it is respectfully submitted that claims 4 and 6 are additionally allowable for these reasons.

With respect to claim 31, this recites "forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å." Due to the use of a "conformal layer" and the "thickness in the range of from 20Å to 70Å", this claim is respectfully submitted to be allowable as respectfully discussed above for these features with respect to claims 1 and 4. Consequently, independent claims 31 and its dependent claims, claims 32-35, are believed allowable. Claim 33 is additionally believed allowable due to the use of the anti-reflective layer which is absent in the Kayanuma reference, as described above with respect to claim 3.

Claim 17 recites performing an anneal prior to forming the insulating layer. The location cited in the Office Action (Wang, col.7, ln. 65, to col. 8, ln. 16) does not recite performing an anneal is only concerning with the forming of a dielectric and not the preceding portions of the process. Claim 17 is additionally believed allowable for this reason.

Claims 37 and 41 are further believed allowable for the recited values of the insulating layer, as described above with respect to claim 4.

Concerning claims 9, 22, and 28, as noted above, both Kayanuma and Takahashi both employ metal silicides that are not anti-reflecting layer. Titanium nitride may be used as an anti-reflective layer, but is not a metal silicide. Consequently, the combination of either of these primary references with the use of titanium nitride in Noda is inconsistent

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

and non-obvious. Therefore, it is respectfully submitted that claims 9, 22, and 28 are further allowable for these reasons.

With respect to claims 10, 23, and 29, the Doan reference recites the use of titanium *silicide*---that is, a metal silicide---and not titanium *nitride*---an anti-reflective layer. As the Office Action notes, the titanium silicide is used to reduce contact resistance, as described above with respect to claim 3, and not for anti-reflective purposes. Therefore, it is respectfully submitted that claims 10, 23, and 29 are further allowable for these reasons.

With respect to claims 11, 24, and 30, the Tsai reference also recites the use of titanium *silicide*---that is, a metal silicide---and not titanium *nitride*---an anti-reflective layer. As the Office Action notes, the titanium silicide is used for its conductive properties, as described above with respect to claim 3, and not for anti-reflective purposes. Therefore, it is respectfully submitted that claims 11, 24, and 30 are further allowable for these reasons.

Conclusion

For any of these reasons, reconsideration of the Office Action's rejection of claims 1-42, is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

EXPRESS MAIL LABEL NO:

EV029354248US

Respectfully submitted,

Michael G. Cleveland
Reg. No. 46,030

2/26/02
Date

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

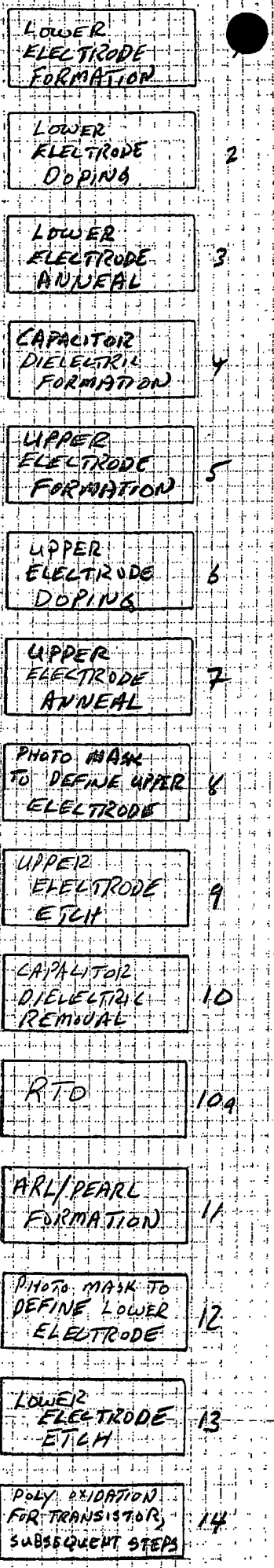
LOWER ELECTRODE FORMATION
1
LOWER ELECTRODE DOPING
2
LOWER ELECTRODE ANNEAL
3
CAPACITOR DIELECTRIC FORMATION
4
UPPER ELECTRODE FORMATION
5
UPPER ELECTRODE DOPING
6
UPPER ELECTRODE ANNEAL
7
PHOTO MASK TO DEFINE UPPER ELECTRODE
8
UPPER ELECTRODE ETCH
9
CAPACITOR DIELECTRIC REMOVAL
10
RTO
10a
ARL/PEARL FORMATION
11
PHOTO MASK TO DEFINE LOWER ELECTRODE
12
LOWER ELECTRODE ETCH
13
POLY OXIDATION FOR TRANSISTORS SUBSEQUENT STEPS
14

FIGURE 12

APPENDIX

Amended Portion of Specification:

The paragraph beginning on page 9, line 1, has been amended as follows:

A preferred embodiment of the present invention is shown in Figure 12 and given by the series of steps:

Standard Submicron Core Technology Flow

1. Lower electrode formation
2. Lower electrode doping
3. Lower electrode anneal

Capacitor Process Module

4. Capacitor dielectric formation
5. Upper electrode formation
6. Upper electrode doping
7. Upper electrode anneal
8. Photo mask to define upper electrode
9. Upper electrode etch
10. Capacitor dielectric removal

10a. RTO

Standard Submicron Core Technology Flow continued

11. ARL/PEARL formation
12. Photo mask to define lower electrode
13. Lower electrode etch
14. Poly oxidation for transistor and subsequent steps,

where steps 9-11 are shown in Figures 2-5. Steps 1-3 and steps 11 on are part of the transistor fabrication process, while steps 4-10a are specific to capacitor formation. These steps differ from the more or less generic prior art by the inclusion of step 10a. The next few paragraphs describe the details of these steps according to this preferred embodiment.

Amended Claim

17.(Amended) The method according to claim 16, wherein prior to forming said insulating layer by deposition, an anneal is performed.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

Pending Claims

1.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer;

subsequently etching said bottom electrode layer.

2.(Amended) The method of claim 1, further comprising forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer and prior to etching said bottom electrode layer.

3.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

forming an anti-reflective layer (ARL) over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.

4.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming an anti-reflective layer (ARL) over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

5. The method according to claim 4, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

6. The method according to claim 5, wherein said thermal process is a rapid thermal oxidation is performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range of from 850°C to 1050°C.

7. The method according to claim 4, wherein said conformal insulating layer is formed by deposition.

8. The method of claim 3, wherein said ARL is an anti-reflective coating.

9. The method of claim 3, wherein said ARL is titanium nitride.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

10. The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. The method according to claim 10, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

12. The method according to claim 2, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

13. A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric.

14. The method of claim 13, further comprising forming a non-insulating layer over at least a portion of the resultant structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer.

15. The method of claim 14, wherein said non-insulating layer is an anti-reflective layer (ARL).

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

16. The method according to claim 15, wherein said insulating layer is formed by deposition.

17.(Amended) The method according to claim 16, wherein prior to forming said insulating layer by deposition, an anneal is performed.

18. The method according to claim 15, wherein said insulating layer is grown.

19. The method according to claim 15, wherein said insulating layer is an oxide layer with a thickness in the range of from 500Å to 2000Å.

20. The method according to claim 15, wherein said side wall spacers have a width in the range of from 500Å to 2000Å.

21. The method according to claim 15, wherein said ARL is an anti-reflective coating.

22. The method according to claim 15, wherein said ARL is titanium nitride.

23. The method according to claim 15, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

24. The method according to claim 23, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

25. The method according to claim 15, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

26. A method of forming a capacitor in an integrated circuit comprising:

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an anti-reflective layer (ARL) over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

27. The method according to claim 26, wherein said ARL is an anti-reflective coating.

28. The method according to claim 26, wherein said ARL is titanium nitride.

29. The method according to claim 26, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

30. The method according to claim 26, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

31. A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer; and

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

32. The method of claim 31, further comprising forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.

33. The method of claim 32, wherein said non-insulating layer is an anti-reflective layer (ARL).

34. The method according to claim 33, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

35. The method according to claim 32, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed in said integrated circuit.

36. A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure;

forming an anti-reflective layer (ARL) over at least a portion of the structure resultant from said forming a conformal layer;

forming a patterned mask over the structure resultant from said forming an ARL; and

etching said conductive layer using said patterned mask.

37. The method according to claim 36, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

38. The method according to claim 37, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28TH Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

39. The method according to claim 36, wherein said conductive layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

40. A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

providing a process flow for etching said conductive layer, whereby the gates of one or more transistors are formed, said flow including a photolithographic process comprising:

forming an anti-reflective layer (ARL) over at least a portion of the conductive layer; and

forming a patterned mask over said ARL, wherein said photolithographic process is optimized for forming said gates;

performing a capacitor formation process comprising:

forming one or more capacitor structures, each comprising a top electrode over a portion of said conductive layer and a dielectric layer between the top electrode and the conductive layer; and

forming a conformal insulating layer over said capacitor structures and at least a portion of said conductive layer proximate to capacitor structures, wherein the capacitor formation process is performed prior to forming said ARL, whereby said ARL is additionally formed over said capacitor structures, and whereby said conformal insulating layer is formed such that said provided process flow is unaltered; and

etching said conductive layer according to said process flow, whereby the lower electrodes of said capacitor structures and said gates are formed.

41. The method according to claim 40, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

42. The method according to claim 41, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646